thickness of each of the leads;

conductive wires for electrically connecting the input/output pads of the semiconductor chip to the leads; and

a package body comprised of an encapsulation material that encapsulates the semiconductor chip, the conductive wires, the chip paddle and the leads, wherein portions of the chip paddle and the leads are externally exposed at a bottom surface of the chip paddle and the leads in the package body.

4. (Twice Amended) The semiconductor package as set forth in claim 1, wherein:

the lower surface of the chip paddle and the lower surface of each of the leads are in a common plane.

6. (Twice Amended) The semiconductor package as set forth in claim 1, wherein:

each of the leads has an etched part at an end facing the chip paddle.

7. (Twice Amended) The semiconductor package as set forth in claim 1, wherein:

the lower surfaces of the leads are externally exposed in the package body.

13. (Four Times Amended) A packaged semiconductor, comprising:

a chip paddle adapted to receive a semiconductor chip, said chip paddle having an upper surface, a lower surface, and an intermediate surface positioned between and parallel to the upper surface and the lower surface;

a plurality of leads surrounding the chip paddle, the chip paddle and the leads comprising a leadframe wherein the intermediate surface of the chip paddle and at least one portion of an upper surface of each of the leads are in approximately a common plane, and wherein the chip paddle has a maximum thickness which exceeds a maximum thickness of

each of the leads; and

the leadframe being adapted to receive a package body comprised of encapsulation material for encapsulating the chip paddle and the leads, wherein portions of the chip paddle and the leads are externally exposed in the package body.

17. (Twice Amended) The packaged semiconductor as set forth in claim 13, wherein:

each of the leads has an etched part at an end facing the chip paddle.

18. (Twice Amended) The packaged semiconductor as set forth in claim 13, wherein:

each of the leads has a lower surface which is externally exposed in the package body.

19. (Thrice Amended) A package for mounting a semiconductor chip, comprising:

a leadframe, comprising:

a chip paddle, wherein a surface of the chip paddle is externally exposed in the package; and

a plurality of leads surrounding the chip paddle, wherein a surface of each of the plurality of leads is externally exposed in the package;

means for receiving encapsulating material for encapsulating the leadframe;

means for locking the encapsulating means to the chip paddle;

means for providing a fluid path for the encapsulating means during encapsulation of the leadframe; and

said means for locking and said means for providing a fluid path being formed from a void caused by said chip paddle being of a maximum thickness which exceeds a maximum thickness of each of the leads.

25. (Thrice Amended) The package as set forth in claim 21, wherein the etched portion is located inside the package body, a lower surface of the chip paddle and a lower surface of each of the plurality of leads are in approximately a common plane, the chip paddle is bonded to a bottom surface of a semiconductor chip and at least one of the plurality of leads has an etched part at an end facing the chip paddle.